

# BUS

## PC-Support Information Pages for PC Internal Bus Systems

Pin assignments and information for: ISA-Bus Pin Assignment, ISA-Bus Signal Description, EISA-Bus (Pin Assignment), VESA-Local Bus (Pin Assignment), PCI-Bus (Pin Assignment), 30 Pin SIMM Connector, 72 Pin SIMM Connector.

Filename : e\_dta-pc-tech-bus.htm

Location : <http://www.elektroniklager.de/pc-sup>

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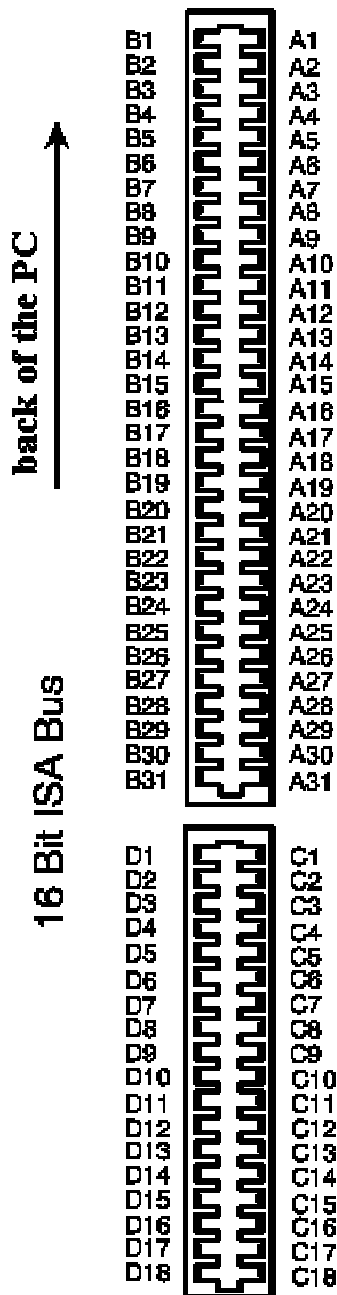
**Revision History:**

Date	Version	Revision	Name	Department	Phone	Description of Changes
2004-06-01	1.0	a	Eberhard De Wille	pc-sup	-	First version of the bus page

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### 1. ISA-Bus



### 1.1. ISA-Bus Pin Assignment at the Slot

#### 62-Pin Slot

Ground	<	B1	A1	<	-I/O CH CK
+ Reset	<	B2	A2	<>	SD7
+5 Volts	<	B3	A3	<>	SD6
+IRQ2(IRQ9/XT)	>	B4	A4	<	SD5
-5 Volts	<	B5	A5	<>	SD4
+ DRQ2	>	B6	A6	<	SD3
-12 Volts	<	B7	A7	<>	SD2
-OWS	<>	B8	A8	<	SD1
+12 Volts	<	B9	A9	<>	SD0
Ground	<	B10	A10	<	I/O CH RDY
-SMEMW	<	B11	All	<>	AEN
-SMEMR	<	B12	A12	<>	SA19
-IOW	<>	B13	A13	<>	SA18
-IOR	<>	B14	A14	<>	SA17
-DACK3	<>	B15	A15	<>	SA16
+DRQ3	<>	B16	A16	<>	SA15
-DACK1	<>	B17	A17	<>	SA14
+DRQ1	<>	B18	A18	<>	SA13
-REFRESH	<>	B19	A19	<>	SA12
CLK	<>	B20	A20	<>	SA11
+ IRQ7	<>	B21	A21	<>	SA10
+ IRQ6	<>	B22	A22	<>	SA9
+ IRQ5	<>	B23	A23	<>	SA8
+ IRQ4	<>	B24	A24	<>	SA7
+ IRQ3	<>	B25	A25	<>	SA6
-DACK2	<>	B26	A26	<>	SA5
+T/C	<	B27	A27	<>	SA4
+BALE (ALE/XT)	<	B28	A28	<>	SA3
+5 Volts	<	B29	A29	<>	SA2
OSC	<	B30	A30	<>	SA1
Ground	<	B31	A31	<>	SA0

#### 36-Pin Slot

-MEMcs16	>	D1	C1	>	SBHE
-I/Ocs16	>	D2	C2	<>	LA23
+IRQ10	>	D3	C3	<>	LA22
+IRQ11	>	D4	C4	<>	LA21
+IRQ12	>	D5	C5	<>	LA20
+IRQ15	>	D6	C6	<>	LA19
+IRQ14	>	D7	C7	<>	LA18
-DACK0	<	D8	C8	<>	LA17
+DRQ0	>	D9	C9	>	-MEMR
-DACK5	<	D10	C10	>	-MEMW
+DRQ5	>	D11	C11	<>	SD08
-DACK6	<	D12	C12	<>	SD09
+DRQ6	>	D13	C13	<>	SD10
-DACK7	<	D14	C14	<>	SD11
+DRQ7	>	D15	C15	<>	SD12
+5 Volts	<	D16	C16	<>	SD13
-MASTER	>	D17	C17	<>	SD14
Ground	<	D18	C18	<>	SD15

The arrows pointing to the PIN-number denote signals which go into the system board (from the slot card to the bus), and vice versa.

< > denotes bi-directional signals.

### 1.2. Description of the Bus Signals

The signal descriptions in this table are for the AT bus. In case of older namings for the PC/XT the descriptions are separately marked. The letter "E" stands for a signal from the slot into the system board. The letter "A" stands for a signal output from the system board to the bus.

Name	E/A	Description
OWS	E	The "Zero Wait State" signal shows the processor that he can terminate the current bus cycle without inserting additional wait states. In order to execute a memory cycle for a 16-bit device without waitstates, the OWS signal has to be derived from an address decoder gate in connection with a read or write command. To execute a memory cycle, after a read or write cycle in connection with an address decoding, for an 8-bit unit with a minimum of 2 waitstates, the OWS signal has to be set active for the duration of one system clock cycle. To read or write commands for an 8-bit unit are active at the falling edge of a system clock cycle. The OWS signal is active-low and should be driven by an open collector or tristate driver with 20mA current capacity.
AEN	A	Address Enable: This line is used to disconnect the processor or I/O devices from the bus to enable a DMA transfer. If the line is active (high) the DMA controller is taking control over the address bus, data bus, read command lines (for memory and I/O) and the write control lines (for memory and I/O).
BALE (ALE)	A	Address Latch Enable: This line is set by the bus controller (8288) and is used on the system board to latch the valid addresses which are output by the processor. It is used by the I/O channels to detect a valid processor address (together with the AEN signal). The processor addresses are latched at the falling edge of the ALE signal.
CLK	A	Bus Clock: is derived by a divider from the oscillator. Originally the bus frequency was 4.77 MHz (1/3 of 12MHz) The bus frequency can be set by the setup of the mainboard. Attention! Many slot cards do not work with a bus frequency above 8MHz.
-DACK0-7 (-DACKI-3)	A	Acknowledge: These lines are used to signal to the peripheral devices, that a DMA request was accepted. (And to refresh the dynamic memory (DACK0 = REFRESH) for the XT).
DRQ1-7 (DRQ0-3)	E	DMA Request 0 to 3 and 5 to 7: With these lines peripheral devices can request a DMA access. The setting of the lines occurs asynchronously. The lines are prioritized differently: DRQ 7 : lowest priority. DRQ 0 : highest priority. A DMA request is triggered by an active "high" level. The DRQ has to be set until the corresponding DACK line becomes active. DRQ0 to DRQ3 are used for 8 bit transfers, DRQ5 to DRQ7 for 16 bit transfers DRQ4 is only used on the system board and is not available on the bus.
I/O CH CHK	E	E/A-Channel Check: This line informs the processor about parity errors which occurred at memory access (input or output). A low level of the signal means that there was an unrecoverable system error.
I/O CH RDY	E	I/O Channel Ready: This line is normally "high" (ready), and is set "low" (not ready) by either the memory or an I/O device to control I/O or memory accesses. This allows slow I/O or memory devices to use an I/O channel without problems. Every slow device has to set this line "low" immediately after reception of a valid address and the the read or write command. It should be kept low for no longer than 10 clock cycles. Cycles for I/O or memory are multiples of the clock cycle.
-I/O CS16	E	16 Bit I/O Chip Select: Marks a bus transfer of a device on the data bus as a 16bit transmission. The signal is active "low".
-IOR	A	I/O Read Command: This command line set a request to an I/O unit to transmit data on the data bus. This line is either set by the processor or the DMA controller. The signal is active "low".
-IOW	A	I/O Write Command: This command line set a request to an I/O unit to receive data from the data bus. This line is either set by the processor or the DMA controller. The signal is active "low".
IRQ2-14 (IRQ2-7)	E	Interrupt Request 2 to 14: These lines show the processor, that an I/O device requests a service. The interrupt lines are prioritized differently: IRQ2 : highest priority IRQ14 : lowest priority An interrupt request is set by driving the interrupt line from "low" to "high". The line has to be set until the processor accepted the request (and started the interrupt service routine).

Name	E/A	Description
LA17-23	E/A	These unlatched signals are used to address the memory in I/O devices of the system. Up to 16MB can be addressed in the system. The signals are only valid, if also the BALE signal is set to "high". LA17 to LA23 are not latched during the CPU cycle and therefore they are not valid for the complete cycle. The purpose of these signals is to generate a memory decoding for a 1 waitstate memory cycle. The decoding has to be latched by the I/O devices at the falling edge of the BALE signal. These signals can be also set by other processors or DMA controllers on the I/O bus.
-MASTER	E	The signal is used in connection with a DRQ line to gain control over the system. A processor or DMA controller on the I/O bus can set an DRQ signal and gets a -DACK signal as a response. After receiving the -DACK signal the processor can drive the -MASTER signal to "low". Through this the I/O processor gains control over the address, data and control lines of the system (Tri-State condition). After the -MASTER signal is set to "low" the I/O processor has to wait for one system cycle before he can take over the control over the address and data lines. He has to wait for additional 2 system cycles before he can output a read or write command. If the -MASTER signal is set to "low" for longer than 15 us a loss of data in the system memory can occur, because the refresh function is deactivated.
-MEMcs16	E	-MEM 16 Chip Select: signals to the system board that the current data transfer is a 16Bit, 1 waitstate transfer. The signal has to be derived from a decoding of the signals LA17 to LA23. The signal should be set by an open collector or tri-state driver with a 20mA current capacity.
-MEMR (AT) -SMEMR (AT/XT)	A	Memory Read Command: This signal line requests the memory to put data on the data bus. -SMEMR is only active if the address decoding is within the lowest 1MB range. -MEMR is active for all memory read accesses. -MEMR can be set by all processors or DMA controllers on the I/O bus. -SMEMR is derived from -MEMR and the decoding of the lowest 1MB memory range. If a processor on the I/O bus wants to set the -MEMR signal, the address lines have to be set for one system cycle before -MEMR is set active. Both signals are active "low".
-MEMW (AT) -SMEMW (AT/XT)	A	Memory Write Command: This signal line requests the memory to read data from the data bus. -SMEMW is only active if the address decoding is within the lowest 1MB range. -MEMW is active for all memory write accesses. -MEMW can be set by all processors or DMA controllers on the I/O bus. -SMEMW is derived from -MEMW and the decoding of the lowest 1MB memory range. If a processor on the I/O bus wants to set the -MEMW signal, the address lines have to be set for one system cycle before -MEMW is set active. Both signals are active "low".
OSC	A	System Clock: 1/8 of the oscillator frequency with a period of 210 ns. (4.77 MHz, pulse width 33%).
-REFRESH	A	This signal is used in the AT to signal a memory refresh. The signal -DACK0 is used in the XT for this purpose. The signal is active "low".
RESET DRV	A	This line is used for the reset or initializing of the system after a power on. The signal is synchronized with the falling edge of the system clock. The signal level is active "high".
SA0-19 (A0-19)	A	Address bits 0 - 19: These lines are used to address the memory and the I/O devices inside the system. The 20 address lines enable the access to 1MB memory. A0 : least significant bit (LSB). A19 : most significant bit (MSB). These lines are either used set the CPU or a DMA-controller. The signal levels are active "high".
SBHE	A	Bus High Enable: signals a data transfer at the upper byte of the data bus (SD8 to SD15). 16Bit devices use SBHE to condition the data buffer for SD8 to SD15. The signal level is active "high".
SD0-15 (D0-7)	E/A	Data bits 0 - 7 and 8 - 15: These lines are the data bus for the processor, memory and I/O devices. D0 : least significant bit (LSB). D7 (D15) : most significant bit (MSB). The signal levels are active "high".
T/C	A	Terminal Count: On this line a pulse is generated if the terminal count of any DMA channel is reached. The signal level is active "high".

The following voltages are available at the I/O slot:

- + 5 Vdc (+/- 5%) Pin B3 and B29
- 5 Vdc (+/-10%) Pin B5
- + 12 Vdc (+/- 5%) Pin B9
- 12 Vdc (+/-10%) Pin B7
- GND (Ground) Pin B1,B10 and B31

## 2. EISA-Bus Pin Assignment at the Slot

Pin	Signal (Printer Circuit Board Side)	Pin	Signal (Component Side)
F1	GND	E1	CMD#
F2	+5V	E2	START#
F3	+5V	E3	EXRDY
F4	---	E4	EX32#
F5	---	E5	GND
F6	ACCESS KEY	E6	ACCESS KEY
F7	---	E7	EX16#
F8	---	E8	SLBURST#
F9	+12V	E9	MSBURST#
F10	M/IO#	E10	W/R#
F11	LOCK#	E11	GND
F12	(reserved)	E12	(reserved)
F13	GND	E13	(reserved)
F14	(reserved)	E14	(reserved)
F15	BE3#	E15	GND
F16	ACCESS KEY	E16	ACCESS KEY
F17	BE2#	E17	BE1#
F18	BE0#	E18	LA31#
F19	GND	E19	GND
F20	+5V	E20	LA30#
F21	LA29#	E21	LA28#
F22	GND	E22	LA27#
F23	LA26#	E23	LA25#
F24	LA24#	E24	GND
F25	ACCESS KEY	E25	ACCESS KEY
F26	LA16	E26	LA15
F27	LA14	E27	LA13
F28	+5V	E28	LA12
F29	+5V	E29	LA11
F30	GND	E30	GND
F31	LA10	E31	LA9
H2	LA6	G2	GND
H3	LA5	G3	LA4
H4	+5V	G4	LA3
H5	LA2	G5	GND
H6	KEY	G6	ACCESS KEY
H7	D16	G7	D17
H8	D18	G8	D19
H9	GND	G9	D20
H10	D21	G10	D22
H11	D23	G11	GND
H12	D24	G12	D25
H13	GND	G13	D26
H14	D27	G14	D28
H15	ACCESS KEY	G15	ACCESS KEY
H16	D29	G16	GND
H17	+5V	G17	D30
H18	+5V	G18	D31
H19	MAKx	G19	MREQx

### 3. VESA-Local Bus (VLB) Pin Assingment at the Slot

Pin	Signal (Printed Circuit Board Side)	Pin	Signal (Component Side)
B1	Dat00	A1	Dat01
B2	Dat02	A2	Dat03
B3	Dat04	A3	GND
B4	Dat06	A4	Dat05
B5	Dat08	A5	Dat07
B6	GND	A6	Dat09
B7	Dat10	A7	Dat11
B8	Dat12	A8	Dat13
B9	Vcc	A9	Dat15
B10	Dat14	A10	GND
B11	Dat16	A11	Dat17
B12	Dat18	A12	Vcc
B13	Dat20	A13	Dat19
B14	GND	A14	Dat21
B15	Dat22	A15	Dat23
B16	Dat24	A16	Dat25
B17	Dat26	A17	GND
B18	Dat28	A18	Dat27
B19	Dat30	A19	Dat29
B20	Vcc	A20	Dat31
B21	Adr31	A21	Adr30
B22	GND	A22	Adr28
B23	Adr29	A23	Adr26
B24	Adr27	A24	GND
B25	Adr25	A25	Adr24
B26	Adr23	A26	Adr22
B27	Adr21	A27	Vcc
B28	Adr19	A28	Adr20
B29	GND	A29	Adr18
B30	Adr17	A30	Adr16
B31	Adr15	A31	Adr14
B32	Vcc	A32	Adr12
B33	Adr13	A33	Adr10
B34	Adr11	A34	Adr08
B35	Adr09	A35	GND
B36	Adr07	A36	Adr06
B37	Adr05	A37	Adr04
B38	GND	A38	WBACK#
B39	Adr03	A39	BEO#
B40	Adr02	A40	Vcc
B41	n/c	A41	BE1#
B42	RESET#	A42	BE2#
B43	DC#	A43	GND
B44	M/ID#	A44	BE3#
B45	W/R#	A45	ADS#
B46	A46		
B47	A47		
B48	RDYRTN#	A48	LRDY#
B49	GND	A49	LDEV&#60;x&#62;#
B50	IRQ9	A50	LREQ&#60;x&#62;#
B51	BRDY#	A51	GND
B52	BLAST#	A52	LGNT&#60;x&#62;#
B53	ID0	A53	Vcc
B54	ID1	A54	ID2
B55	GND	A55	ID3

<b>Pin</b>	<b>Signal</b> (Printed Circuit Board Side)	<b>Pin</b>	<b>Signal</b> (Component Side)
B56	LCLK	A56	ID4
B57	Vcc	A57	LKEN#
B58	LBS16#	A58	LEAD5#

#### 4. PCI-Bus Pin Assignment at the Slot

This German manufacturer - <http://www.bln.de/hkmesssysteme/home3.htm> offers prototype cards (for experiments, and development of own PCI cards)!

The following pin assignment is valid for the PCI cards universal/3.3V/5V and 32/64 bit

Pin	Signal (Printed Circuit Board Side)	Pin	Signal (Component Side)
B1	-12V	A1	TRST#
B2	TCK	A2	+12V
B3	Ground	A3	TMS
B4	TDO	A4	TDI
B5	+5V	A5	+5V
B6	+5V	A6	INTA#
B7	INTB#	A7	INTC#
B8	INTD#	A8	+5V
B9	PRSNT1#	A9	reserved
B10	reserved	A10	+Vi/o
B11	PRSNT2#	A11	reserved
B12	(KEYWAY1)	A12	(KEYWAY1)
B13	(KEYWAY1)	A13	(KEYWAY1)
B14	reserved	A14	reserved
B15	Ground	A15	RST#
B16	CLK	A16	Vi/o
B17	Ground	A17	VNT#
B18	REQ#	A18	Ground
B19	+Vi/o	A19	reserved
B20	AD[31]	A20	AD[30]
B21	AD[29]	A21	+3.3V
B22	Ground	A22	AD[28]
B23	AD[27]	A23	AD[26]
B24	AD[25]	A24	Ground
B25	+3.3V	A25	AD[24]
B26	C/BE[3]#	A26	IDSEL
B27	AD[23]	A27	+3.3V
B28	Ground	A28	AD[22]
B29	AD[21]	A29	AD[20]
B30	AD[19]	A30	Ground
B31	+3.3V	A31	AD[18]
B32	AD[17]	A32	AD[16]
B33	C/BE[2]#	A33	+3.3V
B34	Ground	A34	FRAME#
B35	IRDY#	A35	Ground
B36	+3.3V	A36	TRDY#
B37	DEVSEL#	A37	Ground
B38	Ground	A38	STOP#
B39	LOCK#	A39	+3.3V
B40	PERR#	A40	SDONE
B41	+3.3V	A41	SBO#
B42	SERR#	A42	Ground
B43	+3.3V	A43	PAR
B44	C/BE[1]#	A44	AD[15]
B45	AD[14]	A45	+3.3V
B46	Ground	A46	AD[13]
B47	AD[12]	A47	AD[11]
B48	AD[10]	A48	Ground
B49	Ground	A49	AD[09]

Pin	Signal (Printed Circuit Board Side)	Pin	Signal (Component Side)
B50	(KEYWAY2)	A50	(KEYWAY2)
B51	(KEYWAY2)	A51	(KEYWAY2)
B52	AD[08]	A52	C/BE[0]#
B53	AD[07]	A53	+3.3V
B54	+3.3V	A54	AD[06]
B55	AD[05]	A55	AD[04]
B56	AD[03]	A56	Ground
B57	Ground	A57	AD[02]
B58	AD[01]	A58	AD[00]
B59	Vi/o	A59	+Vi/o
B60	ACK64#	A60	REQ64#
B61	+5V	A61	+5V
B62	+5V	A62	+5V
B63	reserved	A63	Ground
B64	Ground	A64	C/BE[7]#
B65	C/BE[6]#	A65	C/BE[5]#
B66	C/BE[4]#	A66	+Vi/o
B67	Ground	A67	PAR64
B68	AD[63]	A68	AD[62]
B69	AD[61]	A69	Ground
B70	+Vi/o	A70	AD[60]
B71	AD[59]	A71	AD[58]
B72	AD[57]	A72	Ground
B73	Ground	A73	AD[56]
B74	AD[55]	A74	AD[54]
B75	AD[53]	A75	+Vi/o
B76	Ground	A76	AD[52]
B77	AD[51]	A77	AD[50]
B78	AD[49]	A78	Ground
B79	+Vi/o	A79	AD[48]
B80	AD[47]	A80	AD[46]
B81	AD[45]	A81	Ground
B82	Ground	A82	AD[44]
B83	AD[43]	A83	AD[42]
B84	AD[41]	A84	+Vi/o
B85	Ground	A85	AD[40]
B86	AD[39]	A86	AD[38]
B87	AD[37]	A87	Ground
B88	+Vi/o	A88	AD[36]
B89	AD[35]	A89	AD[34]
B90	AD[33]	A90	Ground
B91	Ground	A91	AD[32]
B92	reserved	A92	reserved
B93	reserved	A93	Ground
B94	Ground	A94	reserved

Attention! Pins 63-94 only exist for 64 bit PCI applications. KEYWAY1 exists for universal and 3.3V mainboards. For 5V mainboards this pin is GND. KEYWAY2 exists for universal and 5V mainboards. For 3,3V mainboards this pin is GND.

+Vi/o is 3.3V for 3.3V mainboards, 5V on 5V mainboards, and defines the signals for universal boards.

## 5. 30 PIN SIMM Connector (Single Inline Memory Module)

For "Fast Page Mode SIMM" mit 256kx8 256kx9 1Mx8 1Mx9 4Mx8 4Mx9

Pin	Signal
1	Vcc
2	-CAS
3	DQ0
4	A0
5	A1
6	DQ1
7	A2
8	A3
9	Gnd
10	DQ2
11	A4
12	A5
13	DQ3
14	A6
15	A7
16	DQ4
17	A8
18	A9
19	A10
20	DQ5
21	-WE
22	Gnd
23	DQ6
24	N/C
25	DQ7
26	QP
27	-RAS
28	-CASP
29	DP
30	Vcc

Attention! QP, CASP and DP are not connected for all x8 bit modules. A9 is not connected for 256k modules and A10 is not connected for 256k and 1M modules. The connector socket consists in total of 60 contacts. Each contact is double i.e. present on each side of the SIMM.

## 6. 72 PIN SIMM Connector (Single Inline Memory Module)

For "Fast Page Mode SIMM" with 256k/512k/1M/2M/4M/8M x 32/36 bit

Pin	Signal
1	Gnd
2	DQ0
3	DQ16
4	DQ1
5	DQ17
6	DQ2
7	DQ18
8	DQ3
9	DQ19
10	Vcc
11	N/C
12	A0
13	A1
14	A2
15	A3
16	A4
17	A5
18	A6
19	A10
20	DQ4
21	DQ20
22	DQ5
23	DQ21
24	DQ6
25	DQ22
26	DQ7
27	DQ23
28	A7
29	N/C
30	Vcc
31	A8
32	A9
33	-RAS3
34	-RAS2
35	MP2
36	MP0
37	MP1
38	MP3
39	Gnd
40	-CAS0
41	-CAS2
42	-CAS3
43	-CAS1
44	-RAS0
45	-RAS1
46	N/C
47	-WE
48	N/C
49	DQ8
50	DQ24
51	DQ9
52	DQ25
53	DQ10
54	DQ26

Pin	Signal
55	DQ11
56	DQ27
57	DQ12
58	DQ28
59	Vcc
60	DQ29
61	DQ13
62	DQ30
63	DQ14
64	DQ31
65	DQ15
66	N/C
67	PD1
68	PD2
69	PD3
70	PD4
71	N/C
72	Gnd

Attention! MP0,MP1,MP2 and MP3 is not connectd for all x32 bit modules. A9 is not connected for 256k and 512k modules. A10 is not connected for 256k, 512k, 1M and 4M modules. RAS1 and RAS3 is not connected for 256k, 1M and 4M modules. The connector socket consists in total of 72 contacts. Each contact is double i.e. present on each side of the SIMM.